

FORM PTO-1449				Atty. Docket No. XA-9673A		Appln. No. 10/751,402	
LIST OF DOCUMENTS CITED BY APPLICANT				Applicant Hiroyuki MIZUNO et al.			
				Filing Date HEREWITH		Group	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
SN	AA	4,973,864	11/90	Nogami	307	530	
SN	AB	5,854,562	12/98	Toyoshima et al.	327	55	
SN	AC	5,386,394	1/95	Kawahara et al.	365	208	
SN	AD	5,526,313	1/96	Etoh et al.	365	205	
SN	AE	5,457,657	10/95	Suh	365	205	
SN	AF	4,777,625	10/88	Sakui et al.	365	207	
SN	AG	5,274,598	12/93	Fujii et al.	365	205	
SN	AH	5,495,440	2/96	Asakura	365	149	
SN	AI	5,917,745	6/99	Fujii	365	63	
SN	AJ	5,978,255	11/99	Naritake	365	149	
SN	AK	5,995,403	11/99	Naritake	365	63	
FOREIGN PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
SN	AL	5-109272	4/30/93	JAPAN			abstract
SN	AM	64-1195	1/5/89	JAPAN			abstract
	AN						
	AO						
	AP						
OTHER (including author, title, date, pertinent pages, etc.)							
SN	AQ	Lee, K-C., et al., "Low Voltage High Speed Circuit Designs for Giga-bit DRAMs", 1996 Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 104-105.					
SN	AR	Itoh, Kiyoo, VLSI Memory Design, Baifukan, 1994, pp. 162-163.					
	AS						
Examiner SON DINH				Date Considered 1/7/05			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							